Abstracts

3.3V GPS Receiver MMIC Implemented on a Mixed-Signal, Silicon Bipolar Array (1992 Vol. II [MWSYM])

K.J. Negus, R.A. Koupal, D. Millicker and C.P. Snapp. "3.3V GPS Receiver MMIC Implemented on a Mixed-Signal, Silicon Bipolar Array (1992 Vol. II [MWSYM])." 1992 MTT-S International Microwave Symposium Digest 92.2 (1992 Vol. II [MWSYM]): 1071-1074.

This generic GPS MMIC contains two stages and the dividers, buffers, digital downconversion phase-frequency detector and negative resistance cell required to synthesize both LOs and a TTL system clock. The MMIC operates from a 20 MHz external reference and provides overall conversion gain of about 65 dB from a 1575 MHz RF to a 15 MHz second IF. The 1.8 x 1.8 mm MMIC is implemented on a mixed-signal, silicon bipolar cell array and consumes less than 150 mW from a single 3.3V supply.

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